DKAN0001A

Programmable Logic Controller for Character LCD Modules

23 July 2008

Introduction

This application note provides and discusses a VHDL component for LCD control. The controller manages the initialization and data flow to HD44780 compatible 8-bit interface character LCD modules. It was primarily developed pursuant to the Lumex LCD General Information datasheet. This example VHDL component allows simple LCD integration into practically any programmable logic application. Figure 1 depicts the controller implemented to interface between an LCD module and a user's custom logic.

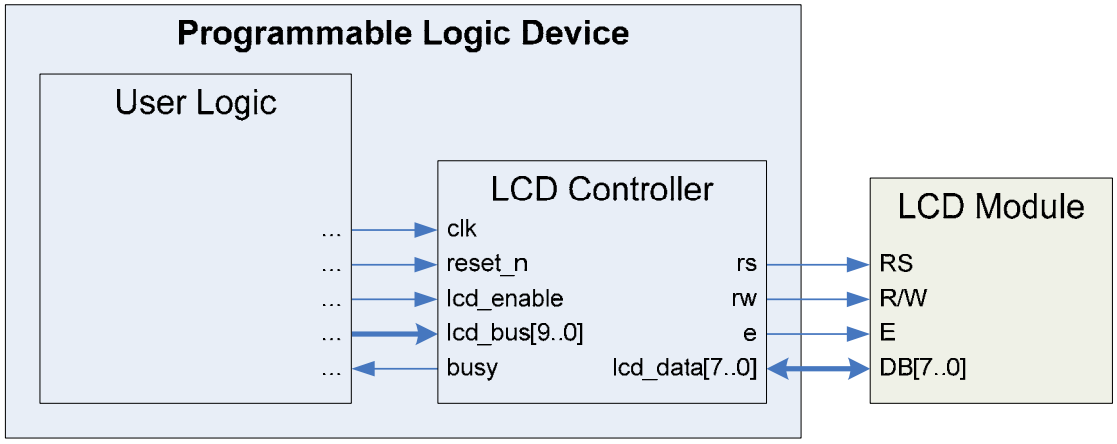

Figure 1. LCD Controller Implementation in PLD

Application

State Machine

The LCD controller consists of five states. Upon startup, it immediately enters the Power-up state, where it waits 50ms to ensure the supply voltage has stabilized. It then proceeds to an Initialize state. The controller cycles the LCD through its initialization sequence, setting the LCD's parameters to default values defined in the hardware. This process completes in approximately 2.2ms, and the controller subsequently assumes a Ready state. It waits in this state until the lcd_enable input is asserted, then advances to the Send state. Here, it communicates the appropriate information to the LCD, as defined by the lcd_bus input. Next, it enters a Busy Check state and continuously polls the LCD to ascertain when its internal operations are complete. Once the controller receives the proper status from the LCD, it returns to the Ready state until further notice. If a low logic level is applied to the reset_n input at any time for a minimum of one clock cycle, the controller resets to the Power-up state and re-initializes. Figure 2 illustrates the LCD controller state machine.

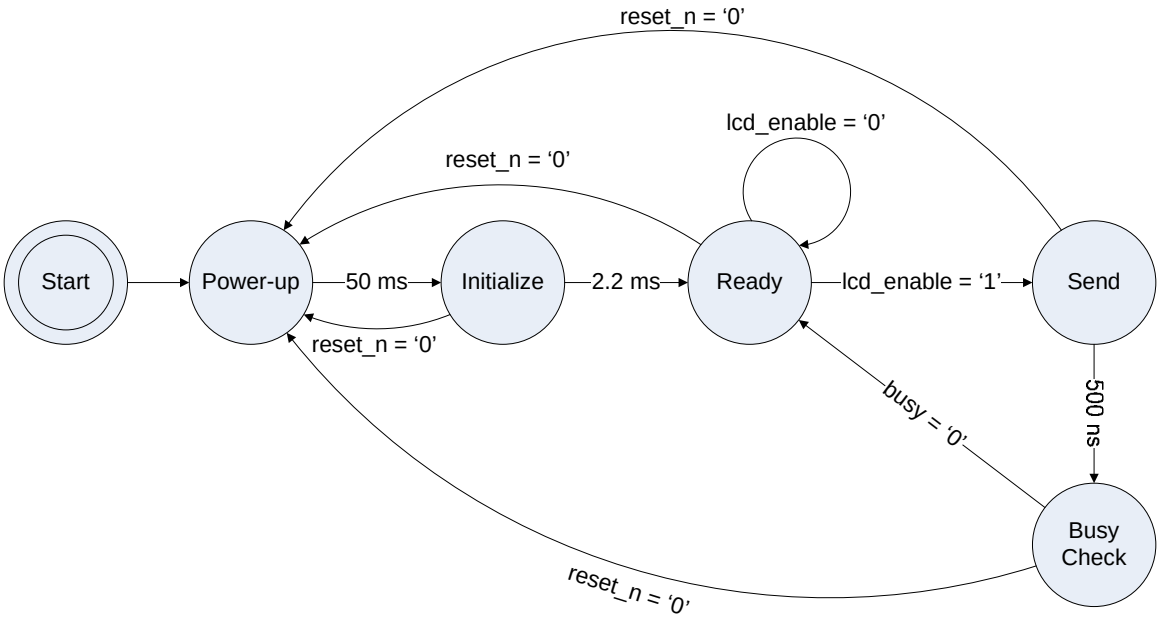

Figure 2. LCD Controller State Machine

Interface

Table 1 describes the LCD controller's I/O pins.

Table 1. LCD Controller I/O Description

I/O Name	Width	Mode	Description	Interface
clk	1	input	Clock for LCD controller. Default set for 50MHz. If a different frequency is desired, change the constant *freq* in the architecture declarations to reflect the new frequency in MHz.	system clock
reset_n	1	input	Active low synchronous reset pin. This pin must be set high to implement the LCD controller. Setting the pin low for one or more clock cycles restarts the LCD controller state machine.	user logic
lcd_enable	1	input	Data latch for LCD controller. H: initiates a transaction using the data currently on the lcd_bus, L: no transaction is initiated and any data on lcd_bus is ignored	user logic
lcd_bus	10	input	Data/instructions to be sent to the LCD module. The MSB is the rs signal, followed by the rw signal. The other 8 bits are the data bits. The LSB on the bus corresponds to the least significant data bit.	user logic
busy	1	output	Feedback on the state of the LCD controller. H: the controller is busy initializing or conducting a transaction with the LCD module, any instructions/data sent will be ignored, L: the controller is idle and ready to accept commands for a transaction	user logic
rs	1	output	LCD module Register Select Signal; H: sending data, L: sending instructions	LCD pin 4
rw	1	output	LCD module Read/Write Select Signal; H: Read, L: Write	LCD pin 5
e	1	output	LCD module enable signal	LCD pin 6
lcd_data	8	bidir	Data bus to the LCD module / busy signal from the LCD	LCD pins 7-14

Initialization

The LCD controller executes an initialization sequence each time it is powered-up or the reset_n pin is deasserted for a minimum of one clock cycle. The controller asserts the busy pin during initialization. Once initialization completes, the busy pin deasserts, and the LCD controller waits in the Ready state for input from the user logic.

The initialization sequence specifies several LCD parameters: function, display control, display clear, and entry mode. The LCD controller instantiates the following default set of these options.

- Function Set: 2-line mode, display on
- Display Control: display on, cursor off, blink off
- Entry Mode: increment mode, entire shift off

The user can send commands to the LCD to change any parameters after initialization. Alternatively, the user can edit the VHDL to change the default parameters. This simply requires commenting out the current VHDL line and uncommenting the line with the desired parameter setting. Table 2 lists the options available in the code.

Table 2. Initialization Options in the VHDL

Option	Choices	VHDL Line	Code
Function Set	2-line mode, display on*	97	lcd_data <= "00111100";
	1-line mode, display on	98	lcd_data <= "00110100";
	1-line mode, display off	99	lcd_data <= "00110000";
	2-line mode, display off	100	lcd_data <= "00111000";
Display ON/OFF	display on, cursor off, blink off*	108	lcd_data <= "00001100";
	display on, cursor off, blink on	109	lcd_data <= "00001101";
	display on, cursor on, blink off	110	lcd_data <= "00001110";
	display on, cursor on, blink on	111	lcd_data <= "00001111";
	display off, cursor off, blink off	112	lcd_data <= "00001000";
	display off, cursor off, blink on	113	lcd_data <= "00001001";
	display off, cursor on, blink off	114	lcd_data <= "00001010";
	display off, cursor on, blink on	115	lcd_data <= "00001011";
Entry Mode Set	increment mode, entire shift off*	131	lcd_data <= "00000110";
	increment mode, entire shift on	132	lcd_data <= "00000111";
	decrement mode, entire shift off	133	lcd_data <= "00000100";
	decrement mode, entire shift on	134	lcd_data <= "00000101";

* denotes default choice

Transactions

Upon deassertion of the busy pin, the LCD controller enters the Ready state. The user logic can interface via the lcd_enable and lcd_bus pins to conduct transactions with the LCD module. The user initiates this process by issuing the desired data/instruction to the lcd_bus and asserting the lcd_enable pin. The LCD controller then asserts the busy pin and manages the transaction. When finished, the controller deasserts the busy pin, indicating that it is ready for another instruction. Figure 3 depicts the timing diagram for the beginning of a transaction.

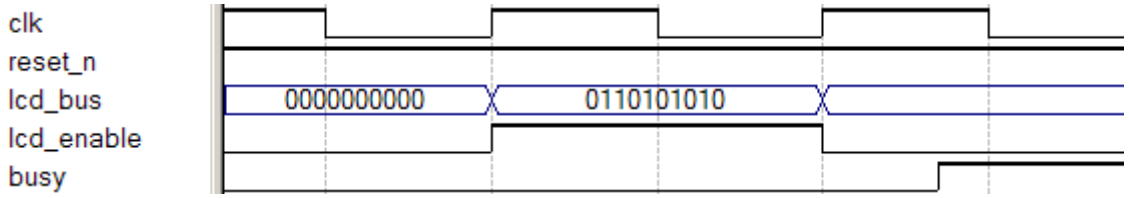

Figure 3. Transaction Timing Diagram

Conclusion

The LCD control logic provided in this application note manages the initialization and data flow between custom user logic and the 8-bit interface mode of HD44780 compatible character LCD modules. The user can set the system clock frequency in the architecture declarations and change the default initialization parameters by selecting which VHDL lines to uncomment.

Additional Information

LCD General Information; Lumex, Inc.

HD44780U (LCD-II); Hitachi, Ltd.

Parts Manufacturers

Digi-Key carries a variety of parts suitable for implementing this LCD controller in programmable logic.

LCDs

8-bit Interface LCD Modules by

- Lumex
- Optrex America
- Varitronix

Programmable Logic

Programmable Logic Devices by

- Altera
- Atmel
- Xilinx

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