



**TEXAS INSTRUMENTS**

Data Sheet  
TI DN 2510477 Rev A  
May 2009

# DLP® Pico Chipset Interface Manual



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## Revision History

<b>Rev</b>	<b>Section</b>	<b>Revisions</b>
A	All	Initial release

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## 1 Glossary

<b>DDR</b>	Double Data Rate
<b>DLP</b>	Digital Light Processing
<b>DMD</b>	Digital Micromirror Device
<b>DVI</b>	Digital Video Interface
<b>FPGA</b>	Field Programmable Gate Array
<b>HVGA</b>	Half VGA (Video Graphics Array), 480x320 Resolution
<b>Pico</b>	Pico Module
<b>PROM</b>	Programmable Read Only Memory
<b>PWM</b>	Pulse Width Modulation
<b>SDRAM</b>	Synchronous Dynamic Random Access Memory

## 2 Related Documents

This section lists related documents associated with the use of the DLP® Pico Chipset. For more information, please visit the [DLPDiscovery.com](http://DLPDiscovery.com).

<b><i>Component Datasheets &amp; Interface Drawings</i></b>	
<b>Document</b>	<b>Drawing #</b>
DLP® Pico Chipset Programmer's Guide	2510328
DLP® PICO™ PROCESSOR DPP1505 DATA SHEET	2510327
DLP® Pico .17 HVGA DDR Series 210 DMD Customer Data Sheet	2510298
.17" HVGA-S210-DMD Mechanical ICD	2509058
DLP Pico Series 210 DMD & System Reference Design: Mechanical and Thermal Application Note	2510323
DLP® Pico Kit Functional Guide	2510476
DLP® Pico MAIN-B SCHEMATIC	2510510
DLP® Pico DVI-B SCHEMATIC	2510511
DLP® Pico DMD-B SCHEMATIC	2510512

### 3 Purpose

This document describes the interface of the Texas Instruments DLP® Pico chipset. The Pico chipset consists of a DPP1505 processor, a PROM, and the .17 HVGA DMD. This document is provided to facilitate use of the chipset.

### 4 Overview

The DLP® Pico chipset offers system developers the ability to design with the DLP technology in a small form factor. The Chipset allow the developer to process light for a variety of applications.

The DLP® Pico Chipset includes the DPP1505 (an FPGA), a Flash memory (PROM1505) to store the program data needed by the DPP1505, and a HVGA .17 DDR DMD.

#### DMD Type

- 0.17" HVGA DMD

#### DPP1505 DLP Pico™ Processor

- Performs all image processing and control
- Performs DMD data formatting
- Control of the 0.17 HVGA DMD

#### PROM

- Contains DPP1505 configuration information

#### **4.1 *Discovery™ 4000 DMD Features***

The DLP® Pico chipset allows very small systems to be developed that are bright, have excellent image quality, and draw very low electrical power. LED current, for controlling LED power, is programmable via command inputs to the projector. Image processing, subsystem control, and DMD data formatting are integrated on to a single integrated circuit (IC), the DPP1505.

## 5 Chipset Components

Figure 1 below is a simplified system block diagram showing the use of the DPP1505 with the following components:

- .17" HVGA DMD – Spatial Light Modulator
- DPP1505 – Altera Cyclone-III FPGA configured to provide high-speed DMD data and control
- PROM – Serial flash PROM which contains startup configuration information for the DPP1505

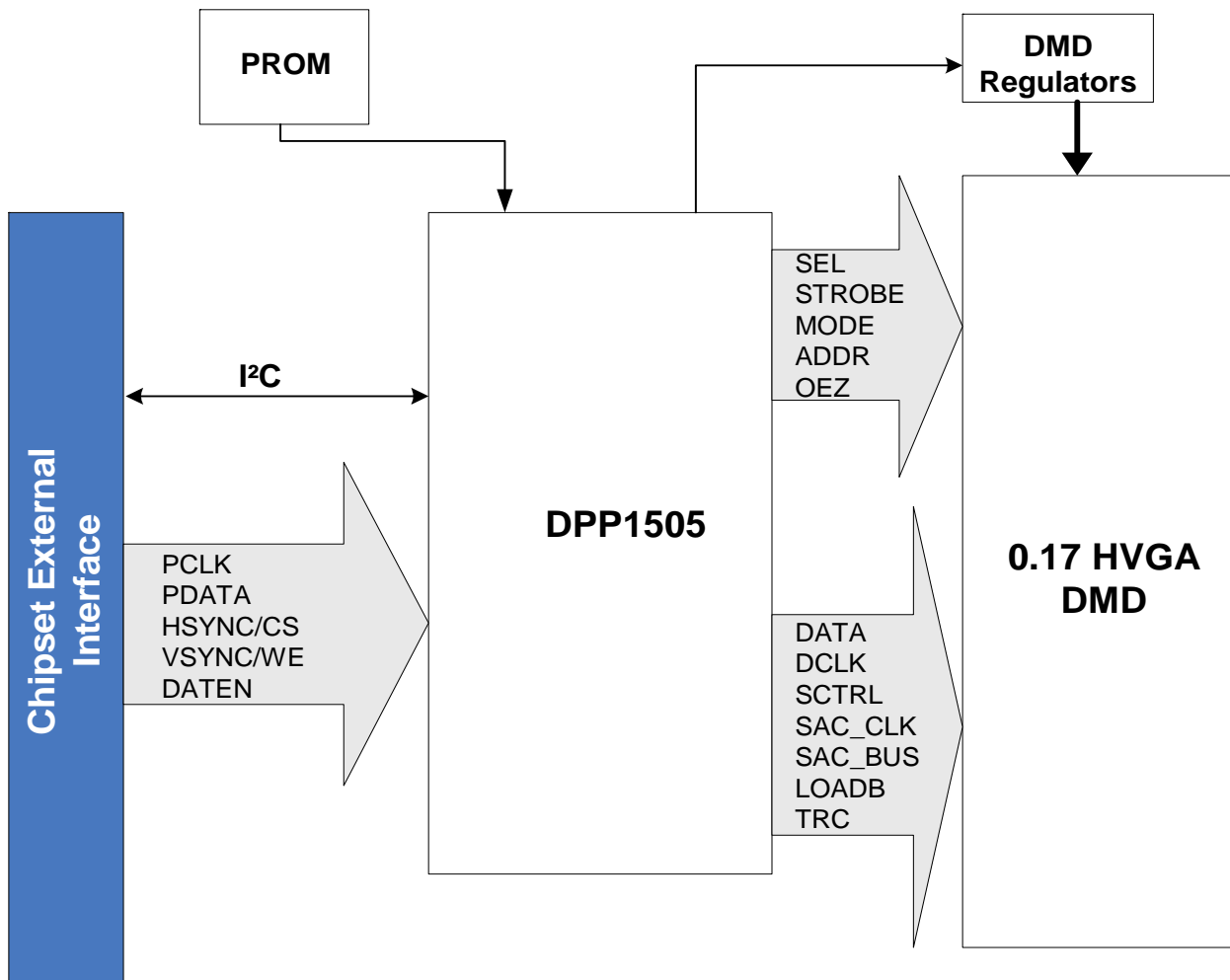


Figure 1 DLP® Pico Chip Set Block Diagram

## 5.1 DPP1505

The DPP1505 is the DLP Pico Processor included in the chipset. The DPP1505 performs Image processing and control, along with DMD data formatting for the 0.17 HVGA DMD. As with prior DLP® electronics solutions, image data is 100% digital from the DPP1505 input port to the image being displayed. The DPP1505 processes the digital input image and converts the data into a format needed by the DMD. The DMD then reflects light to the screen using binary Pulse Width Modulation (PWM) for each pixel mirror. The viewer's eyes integrate this Pulse Width Modulated light to form brilliant, crisp images. Commands can be input to the DPP1505 over the CPU Bus or over the I2C interface.

For more information, refer to the DPP1505 Data Sheet TI DN 2510327.

## 5.2 Flash Configuration PROM

The DPP1505 is configured at startup from a serial flash PROM. The contents of this prom can not be altered.

## 5.3 DMD

The DLP® Pico system includes the .17" HVGA DMD devices.

# 6 DMD Operation

The .17 HVGA DMD in the Pico system is a spatial light modulator which consists of a 320 (H) x 480 (V) array of Micromirrors. In this device, data is clocked into the DMD on both the Rising and Falling Edges of DCLK. This is referred to as Double Data Rate (DDR).

In the Pico system, the DPP1505, which controls the periodic refreshes of the DMD, provides the data output in a format required by the DMD. The DMD then reflects light using Pulse-Width-Modulation (PWM). The viewers' eyes integrate this light to form brilliant, crisp images.

## 7 DLP® Pico Interfaces

This section shows the interface between the different components included in the chipset.

### 7.1 User to DPP1505 Interface

#### 7.1.1 DPP1505 IO Description

Table 1 below describes the inputs and outputs of the DPP1505. The DPP1505 provides a single image input port. The signals listed below support three input interface modes, thus some signals have different uses depending on the input interface mode being used. The three input image interface mode options are the Parallel Bus, CPU Bus, or BT.656.

**Table 1 DPP1505 Input/Output Description**

Pin Name	Parallel RGB	BT.656	CPU I/F	I/O
PCLK	Clock	Clock	Read enable (Not used)	I
VSYNC_WE	Vsync	Unused	Write enable (active low)	I
HSYNC_CS	Hsync	Unused	Chip select (active low)	I
DATEN_CMD	Active data	Unused	RA0 (active low)	I
CPUVSYNC	Unused	Unused	TE sync	O
PDATA[0]	Data	Data0	Data	I
PDATA[1]	Data	Data1	Data	I
PDATA[2]	Data	Data2	Data	I
PDATA[3]	Data	Data3	Data	I
PDATA[4]	Data	Data4	Data	I
PDATA[5]	Data	Data5	Data	I
PDATA[6]	Data	Data6	Data	I
PDATA[7]	Data	Data7	Data	I
PDATA[8]	Data	Unused	Data	I
PDATA[9]	Data	Unused	Data	I
PDATA[10]	Data	Unused	Data	I
PDATA[11]	Data	Unused	Data	I
PDATA[12]	Data	Unused	Data	I
PDATA[13]	Data	Unused	Data	I
PDATA[14]	Data	Unused	Data	I

Pin Name	Parallel RGB	BT.656	CPU I/F	I/O
PDATA[15]	Data	Unused	Data	I
PDATA[16]	Data	Unused	Data	I
PDATA[17]	Data	Unused	Data	I
PDATA[18]	Data	Unused	Data	I
PDATA[19]	Data	Unused	Data	I
PDATA[20]	Data	Unused	Data	I
PDATA[21]	Data	Unused	Data	I
PDATA[22]	Data	Unused	Data	I
PDATA[23]	Data	Unused	Data	I

## 7.2 DPP1505 to DMD Interface

### 7.2.1 DPP1505 to DMD IO Description

The DPP1505 has a DDR DMD interface for sending image data to the DMD. The bus width is 10 bits. A 60MHz clock is used for this image interface. One 10-bit image word is capture by the DMD on each rising and falling edge of the clock. Several DMD control signals are also output from the DPP1500 to the DMD.

The interface signals, for both image and control, use 1.8V switching levels.

Table 2 lists the signal names that make up the .17 DMD interface and their corresponding types.

**Table 2 DPP1505 to DMD I/O Pin Descriptions**

Pin Name	DESCRIPTION	I/O
DMD_D0	DMD Data Pins. DMD Data pins are DDR (Double Data Rate) signals that are clocked on both edges of DMD_DCLK	O
DMD_D1		
DMD_D2		
DMD_D3		
DMD_D4		
DMD_D5		
DMD_D6		
DMD_D7		
DMD_D8		
DMD_D9		
DMD_DCLK	DMD Data clock.	O
DMD_LOADB	DMD Data Load Signal.	O

Pin Name	DESCRIPTION	I/O
DMD_SCTRL	DMD Data Serial Control Signal.	O
DMD_TRC	DMD Data Toggle Rate Control.	O
DMD_A0	DMD Reset Address.	O
DMD_A1		
DMD_A2		
DMD_SEL0	DMD Reset Selection.	O
DMD_SEL1		
DMD_MODE	DMD Reset Mode.	O
DMD_STROBE	DMD Reset Strobe.	O
DMD_SACBUS	DMD Serial Bus Data.	O
DMD_SACCLK	DMD Serial Bus Clock.	O
DMD_OEZ	DMD Reset Output Enable. (Active Low)	O
DMD_PWR_EN	DMD Power Regulator Enable. (Active high)	O

### 7.2.2 DMD Regulators

The DMD\_PWR\_EN signal from the DPP1505 enables the DMD regulators that create the VRST, VBIAS, and VOFS voltages. These are three distinct voltage levels needed by the DMD.

Figure 2 Shows the DMD regulator interface from the DPP1505.

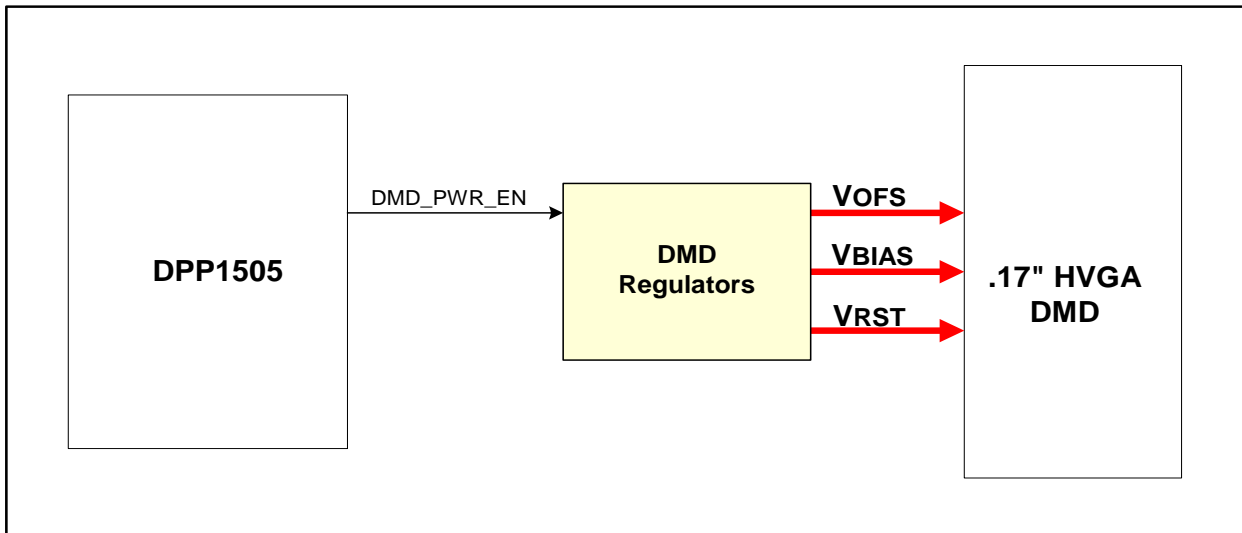


Figure 2 DMD Regulator Interface

### 7.3 Power-Up Sequence

- (1) Power supplies #1 - #N are all of the power supplies (P2P5V, P1P8V, P1P2V, INTFPWR, FLASHPWR, and P3P3V). For the LED driver and the DMD power supplies (VRST, VBIAS, VOFS), the module will internally handle sequencing on of these power supplies as needed.
- (2) Power supplies (#1 - #N) can sequence on in any order as long they all turn on (are stable and within spec) within a 3ms time window.
- (3) 1.0 second max after PWRGOOD goes high the module begins to operate using the default configuration settings from the Flash. After 1.0 second min from PWRGOOD going high, commands can be input to the module.
- (4) I2C reads/writes and CPU bus writes to the DPP1505 are invalid before 1.0 second after PWRGOOD. I2C signals and the CPU bus chip select (HSYNC\_CS) should all be high before 1.0 second after PWRGOOD including for reads/writes to other devices.

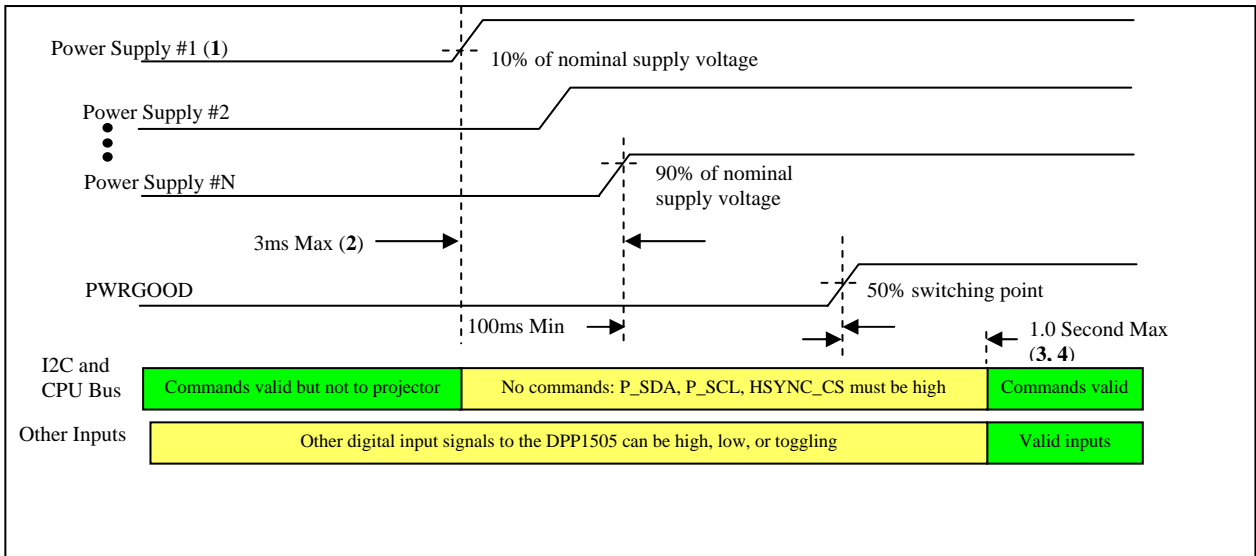


Figure 3 Power-Up Sequence

## 7.4 LED Driver Interface

The DPP1505 outputs three enables for turning on and off the three LEDs (R, G, B). The LED enables will automatically turn on and off to create the R, G, and B duty cycles desired over each image frame. The duty cycles are controlled by the DPP1505

The LED current for each LED is programmable in the DPP1505. The LED current can be set over the I2C bus. The DPP1505 controls currents by sending three PWM waveforms to the LED Driver circuit.

Figure 4 shows the LED driver interface from the DPP1505.

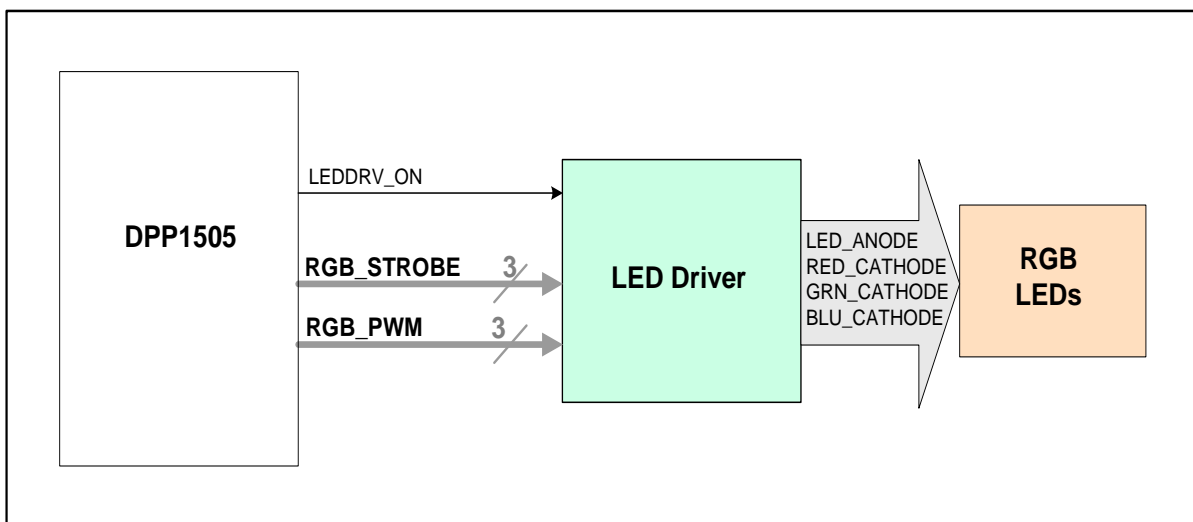


Figure 4 LED Driver Interface

The three main set of signals are the LEDDRIV\_ON which is used to turn the he LED Driver on or off. The RGB\_PWM signals control the current (100mA ~ 750mA) of the red, green, and blue LEDs. The RGB\_STROBE signals enable the red, green, and blue LEDs.

For the LED Driver a max value of PWM duty cycle gives the minimum current setting.

**Table 3 DPP1505 to LED Driver I/O Pin Descriptions**

<b>Pin Name</b>	<b>DESCRIPTION</b>	<b>I/O</b>
BLU_PWM	Blue LED PWM signal used to control the LED Current.	O
RED_PWM	Red LED PWM signal used to control the LED Current.	O
GRN_PWM	Green LED PWM signal used to control the LED Current.	O
BLU_STROBE	Blue LED Enable.	O
RED_STROBE	Red LED Enable.	O
GRN_STROBE	Green LED Enable.	O
LED_FAULTZ	LED Fault indication. Signal forces LEDDRV_ON low and RGB Strobes low (active low)	I
LED_ENABLE	LED Enable. Signal forces LEDDRV_ON low and RGB Strobes low.	I
LEDDRV_ON	LED Driver Enable.	O

## 8 Power Supply Interface

Power supply inputs for the Pico module.

**SYS\_PWR:** The voltage range is 4.5V to 5.5V. SYS\_PWR is from the DC power supply input to the Pico module. The supply is distributed to the LED driver circuit and the DMD regulators that create VOFS, VRST, and VBIAS.

**P2P5V:** This is the 2.5V and is the supply for The DMD core voltage, the DPP1505 DLL, and the LED control circuit.

**P1P8V:** This is the 1.8V and is the I/O supply for the DPP1505, the SDRAM memory and the DMD.

**P1P8V:** The 1.8V supply proves the core voltage for the DPP1505.

**INTFPWR:** For switching voltage of I/O signals on the DPP1505. Allows switching between 3.3V and 1.8V. Default setup of the schematic is set to 3.3V.

**FLASH\_PWR:** For setting the FLASH supply voltage between 3.3V and 2.5V. Default setup of the schematic is set to 3.3V.

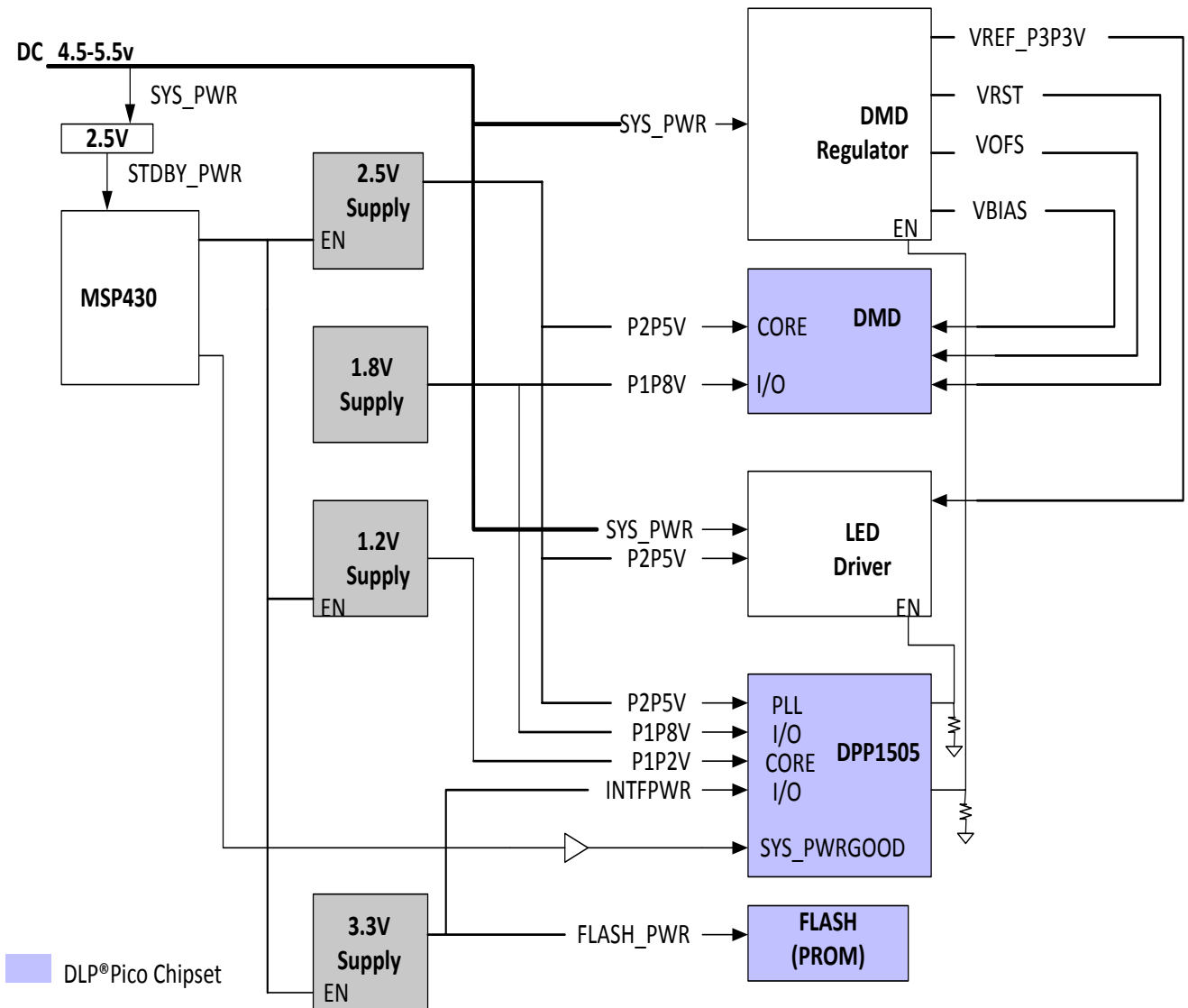


Figure 5 Power Supply Interface

**Pico Projector Recommended Operating Conditions**

Below are the operating voltage and current for the Pico module supply.

Parameter	Min.	Nom.	Max.	Unit
DC supply voltage	4.5	5	5.5	V
DC supply Current	1000@5V			mA

**I/O Specification of the HDMI Interface**

Below are the signal specifications of the I/O Interface for the external interface of the Pico kit.

**Input I/O Voltage Range - Logic signals**

Parameter	Min.	Nom.	Max.	Unit
High-level Input Signal Voltage	2		3.3	V
Low-level Input Signal Voltage	0		0.8	V

**Input I/O Voltage Range - Differential signals**

Parameter	Min.	Nom.	Max.	Unit
Differential Input Voltage Single Ended Amplitude (TMDS)	75		1000	mV