Data Sheet
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DLP® Pico Kit Functional Guide

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Revision History

Rev	Section	Revisions
A	All	Initial release

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1 Reference

1. DLP® Pico Chipset Programmer's Guide, TI drawing number 2510328
2. DLP® PICO™ Processor DPP1505 Data Sheet, TI drawing number 2510327
3. DLP® Pico Chipset Interface Manual, TI drawing number 2510477
4. DLP® Pico .17 HVGA DDR Series 210 DMD Customer Data Sheet, TI drawing number 2510298
5. DLP® Pico MAIN-B SCHEMATIC, TI drawing number 2510510
6. DLP® Pico DVI-B SCHEMATIC, TI drawing number 2510511
7. DLP® Pico DMD-B SCHMATIC, TI drawing number 2510512

2 Function Purpose

This document is intended to describe the expected use and configurations of the DLP® Pico Kit. Once the Pico kit is setup, the user will be able to display content out of the Pico module.

The DLP® Pico Development Kit enables developers to integrate this light modulating technology into their applications with the benefits of a small form factor. All image processing, subsystem control, and DMD data formatting is integrated on to a single integrated circuit. The chipset which includes the DPP1505, the Flash memory (PROM), and a HVGA .17 DMD is housed in the Pico module.

3 Theory of Operations

The Pico module is compatible with the Beagleboard. The Pico-Beagle configuration is shown in Figure 1 below. The Pico Development kit includes the Pico module, a Power supply, and a custom HDMI cable. A USB to Mini-USB cable can be used to power the Beagle Board, and an SD card enables access to video content.

For instructions on how to format the SD Card go to http://beagleboard.org/pico.

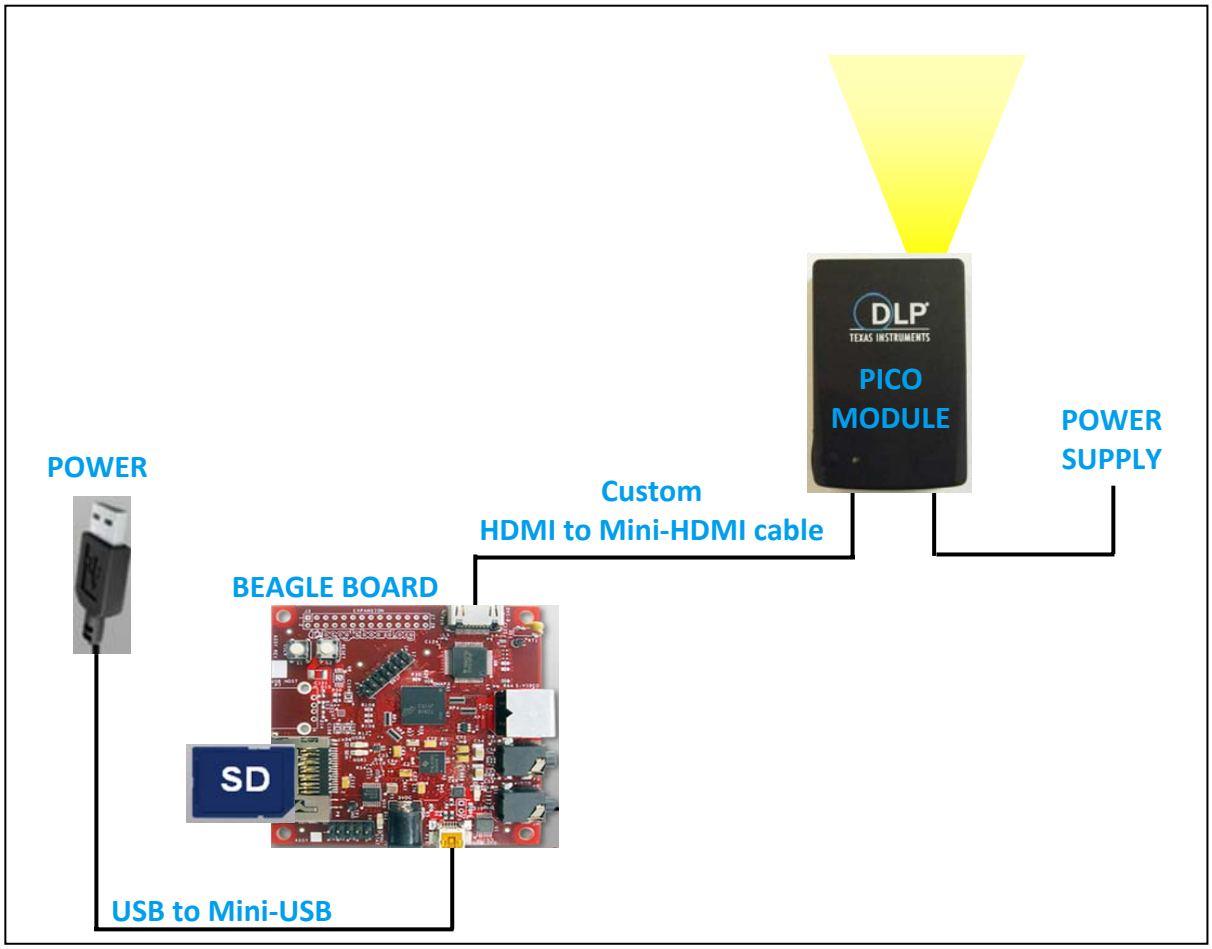


Figure 1: Pico Development Kit Setup

The Pico module can display the output from the Beagleboard. The Beagleboard needs to be configured in VGA display mode in order to interface to the Pico. A VGA-based Beagleboard SD card configuration is available for download. The SD card is configured with a video demo that starts when the Beagleboard completes booting up.

3.1 Basic features

With the Pico system, still images and motion can be displayed in RGB mode. There is also an internal test pattern feature that diplays pre-defined test patterns. The third option is the splash screen mode which displays stored Splash Screen images. Table 1 showes the three modes of operation and there assiciated input information.

Table 1: Pico input image operation

	RGB mode	**Test Pattern**	**Splash screen**
Input Source and Interface Mode	Parallel I/F	Internal Test Patterns	Splash screen
Input Resolution	VGA	HVGA	QVGA
Pixel Format	RGB565/RGB666/ RGB888	RGB888	RGB565
Frame Rate	50-60Hz	-	-

3.2 System Level Hardware Theory of Operation

The DLP® Pico system offers developers light processing in a small form factor. The Pico module allows very small projection and is bright, with excellent image quality. LED current, for controlling LED power, is programmable via command inputs to the projector.

Figure 2 shows a block diagram of the DPP1505, PROM1505, and HVGA .17 DMD as used in the Pico Development Kit. The user interface is a HDMI input into the Pico module.

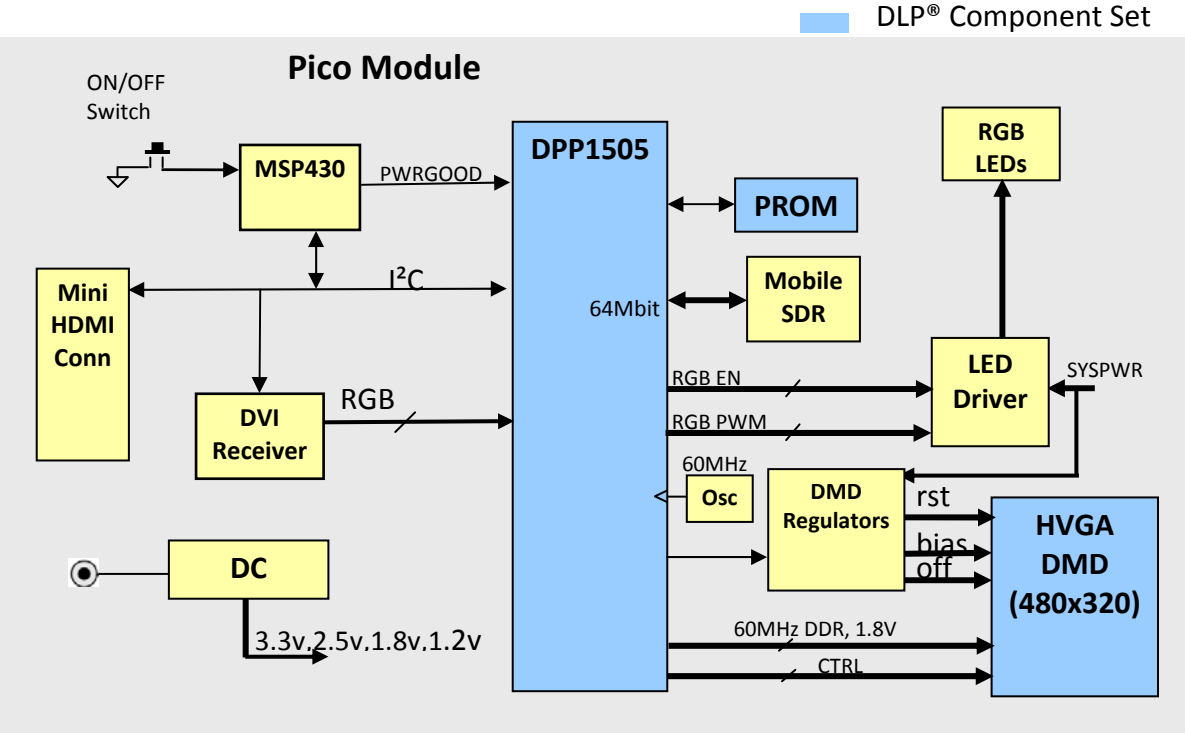


Figure 2: Pico System Block Diagram

3.2.1 DLP® Pico Components

DPP1505:
The DPP1505 provides one 24-bit port for images being input from an MPU, from a video decoder, or from other peripheral devices such as a card reader. These various devices can be tri-state multiplexed into this input port. In the case of the Pico Kit module images are input from a DVI receiver as shown in Figure 2 above.

The DPP1505 accepts up to 60Hz VGA image resolutions. The DPP1505 provides a single input port for graphics and motion inputs. The input port can be configured as a Parallel Bus, a CPU Bus, or for BT.656 for motion. The signals on this port have different uses depending on the interface mode being used. Figure 3 shows how how these signals are shared.

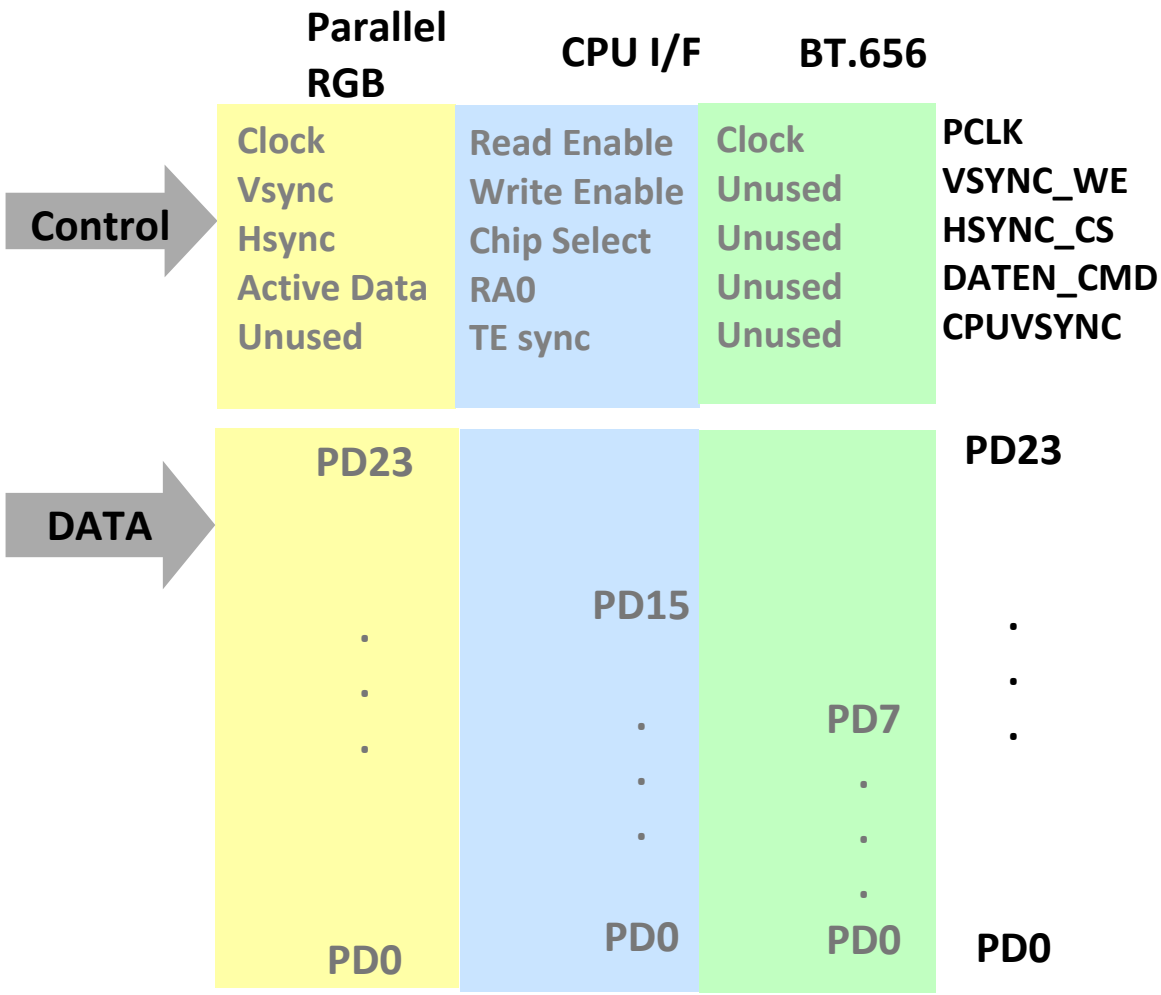


Figure 3: DPP1505 Input Port

PROM:
The flash prom for the DPP1505 stores the program data needed by the DPP1505 Pico processor chip. The contents of this prom can not be altered.

HVGA DMD:

The .17 HVGA DMD in the Pico system is a spatial light modulator which consists of a 320 (H) x 480 (V) array of Micromirrors. In this device, data is clocked into the DMD on both the Rising and Falling Edges of DCLK.

3.2.2 System Power Distribution

Power supply inputs for the Pico module.

SYS_PWR:
The nominal voltage is 5V. SYS_PWR is from the DC power supply input to the Pico module. The supply is distributed to the LED driver circuit and the DMD regulators that create VOFS, VRST, and VBIAS.

P2P5V:
This is the 2.5V and is the supply for The DMD core voltage, the DPP1505 DLL, and the LED control ciruit.

P1P8V:
This is the 1.8V and is the I/O supply for the DPP1505, the SDRAM memory and the DMD.

P1P8V:
The 1.8V supply proves the core voltage for the DPP1505.

INTFPWR:
For switching voltage of I/O signals on the DPP1505. Allows switching between 3.3V and 1.8V. Default setup of the schematic is set to 3.3V.

FLASH_PWR:
For setting the FLASH supply voltage between 3.3V and 2.5V. Default setup of the kit is set to 3.3V.

Figure 3 shows the power distribution for the Pico module.

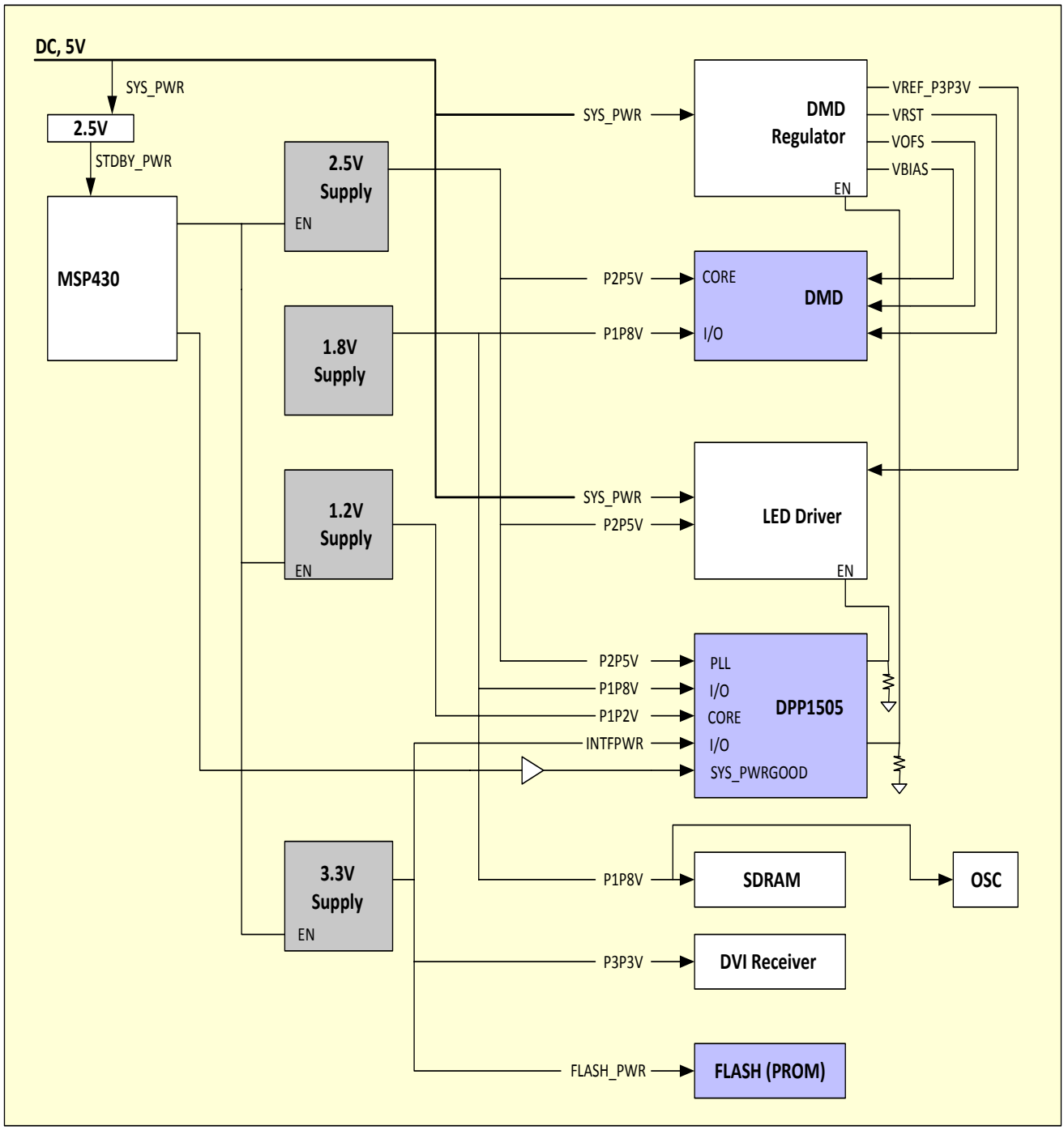


Figure 4: Power Distribution for the Pico Kit

Pico Projector Absolute Maximum Ratings

Parameter	Min.	Nom.	Max.	Unit
DC supply voltage	-0.3	-	6	V

Pico Projector Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Unit
DC supply voltage	4.5	5	5.5	V
DC supply Current	1000@5V			mA

I/O Specification of the HDMI Interface
Below are the signal specifications of the I/O Interface for the external interface of the Pico kit.

Input I/O Voltage Range - Logic signals

Parameter	Min.	Nom.	Max.	Unit
High-level Input Signal Voltage	2		3.3	V
Low-level Input Signal Voltage	0		0.8	V

Input I/O Voltage Range - Differential signals

Parameter	Min.	Nom.	Max.	Unit
Differential Input Voltage Single Ended Amplitude (TMDS)	75		1000	mV

3.3 Limitations & Assumptions

The Pico kit was developed to work with the Beagle Board. The Beagle Board provides input to the Pico module through the HDMI interface.

3.4 Full System configuration considerations

The Pico kit was designed to connect to the Beagle Board. To display content on the Pico module, the following steps are necessary.

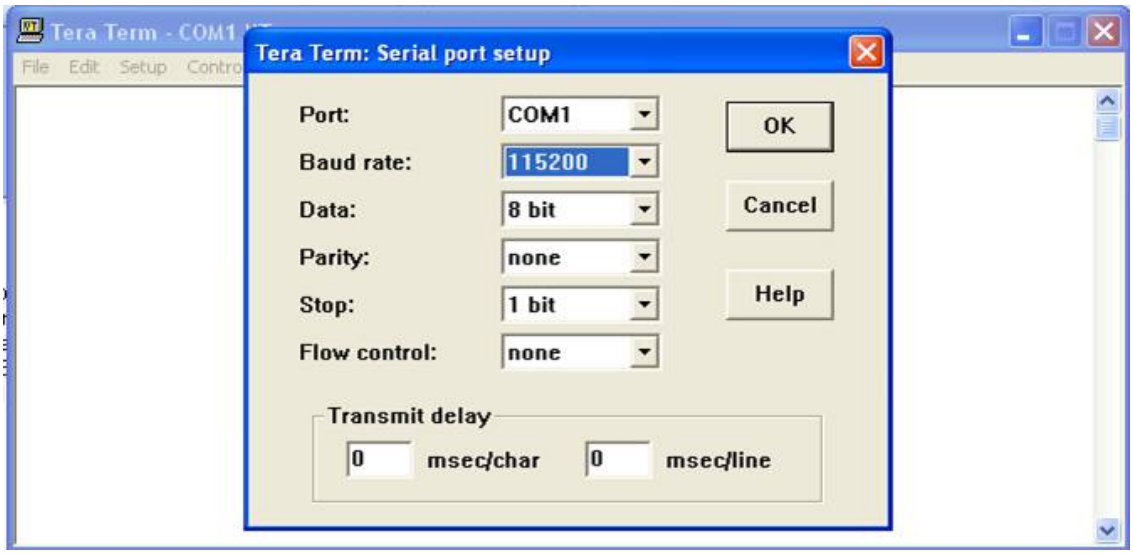
Connect the Pico module to the Beagle board according to Figure 1, and display content from an SD card that is loaded on the beagle board.

A 2GB (or greater) SD card can be configured or a pre-configured SD card may be purchased (see the http://beagleboard.org/pico page to configure and SD card or purchase one)

Once you have the Configured SD card then you can follow the steps below to get content to play on the Pico.

You will need to do steps 1 through 7 the first time you use the Beagle board with a pre-configured SD card. After performing these steps the content on the SD card will start playing at boot up with this Beagle Board without being connected to a PC.

1. Connect the power supply to the Pico.
2. Connect a serial cable to your PC and the RS232 connector on the beagle Board.
3. Turn on the Pico. (wait until step five to connect power to the Beagle Board)
4. Open Tera Term Pro and select the Serial, port: COM1 (for the New Connection)
5. Go to Setup (top of the window) and select serial port... You will see a number of selections on the Serial port setup pop-up window. configure as follows: BAUD RATE - 115200, DATA - 8 bit, PARITY- none, STOP - 1bit, FLOW CONTROL – none.



6. Plug in the Beagle Board power (USB cable) and boot the Beagleboard with your configured SD card. You should see something like what is shown below in the TeraTerm display.

Texas Instruments X-Loader 1.41
Starting OS Bootloader...

U-Boot 1.3.3 (Jul 10 2008 - 16:33:09)

OMAP3530-GP rev 2, CPU-OPP2 L3-165MHz
OMAP3 Beagle Board + LPDDR/NAND
DRAM: 128 MB
NAND: 256 MiB
In: serial
Out: serial
Err: serial
Audio Tone on Speakers ... complete
OMAP3 beagleboard.org #

7. At the prompt #, enter the following commands. The Beagleboard will automatically boot from the SD card the next time it is reset.

```
# setenv bootargs 'console=ttyS2,115200n8 console=tty0 root=/dev/mmcblk0p2 rw
    rootfstype=ext3 rootwait'
# setenv bootcmd 'mmcinit;fatload mmc 0 80300000 uImage;bootm 80300000'
# saveenv
# run bootcmd
```

8. The next time the Pico kit boots up with the configured SD card the content will automatically be displayed out of the Pico. Apply power to the Pico then apply power to the Beagle Board once the BeagleBoard icon appears it will take a few seconds before the content starts playing on the Pico.

3.5 Parameter Considerations

When bringing up the Pico-Beagle System in order to display an image from the Beagle board onto the Pico module the Beagle board must be powered on last.

All the commands needed to setup the Pico module in different modes are described in the "DLP® Pico Chipset Programmer's Guide" document which can be found on page www.dlpdiscovery.com/pico. Below is a highlight of some setting that are mode (motion, test patterns, etc.) dependant.

The power-on default settings for the Pico module are as follows. When the Pico module boots up, a splash screen image with the Texas Instruments logo will be displayed.

Table 4: Default Settings

	Default Settings	**I2C Command Register (Addr)**
Input Source and Interface Mode	Parallel RGB I/F	0x04
Degamma Curve	Enhanced Graphics	0x1E
Mode Select	60Hz Mode	0x1F
Sync Mode	Lock to internally generated sync	0x24
Temporal Enhance	Disabled	0x26
Internal Test Patterns	Checkerboard	0x0B
Red LED Driver Current	Maximum value	0x0E
Green LED Driver Current	Maximum value	0x0F
Blue LED Driver Current	Maximum value	0x10

RGB Mode:
When playing video from the Beagle board it is best to enable the features that will enhance the image in this mode. The settings in Table 5 are recommended for the RGB mode.

Table 5: RGB Mode Settings

	RGB Mode	I2C Command Register (Addr)
Input Source and Interface Mode	Parallel RGB I/F	0x04
De-gamma Curve	Enhanced Graphics	0x1E
Mode Select	60Hz Mode should be used for NTSC inputs and the 50Hz Mode is for PAL/SECAM support	0x1F
Sync Mode	for valid image inputs with frame rates of 50-60Hz, and input frames are periodic “Lock to incoming sync” mode should be used	0x24
Temporal Enhance	The Temporal Enhance feature should be enabled in video mode to improve image quality	0x26

Test Pattern Mode:

For internal test pattern usage, the command settings in Table 6 should be used.

Table 6: Test Pattern Mode Settings

	Test Pattern Mode	I2C Command Register (Addr)
Input Source and Interface Mode	Internal Test Patterns	0x04
De-gamma Curve	Enhanced Graphics	0x1E
Mode Select -	60Hz Mode	0x1F
Sync Mode - Lock to internally generated sync	Lock to internally generated sync mode should be selected if there is no external VSYNC	0x24
Temporal Enhance	Disabled	0x26
Internal Test Patterns	Desired test pattern*	0x0B

*Select desired test pattern from the list of Internal Test Patterns.

When displaying user defined patterns or images; use the following settings to eliminate the impact of the video enhancement features.

Table 7: Setting options for custom images

	Custom patterns*	**I2C Command Register (Addr)**
Input Source and Interface Mode	Parallel RGB I/F	0x04
De-gamma Curve	There is a Linear degamma that can be selected	0x1E
Mode Select	60Hz Mode should be used for NTSC inputs and the 50Hz Mode is for PAL/SECAM support	0x1F
Sync Mode	for valid image inputs with frame rates of 50-60Hz, and input frames are periodic “Lock to incoming sync” mode should be used	0x24
Temporal Enhance	Disabled	0x26
AGC (Automatic Gain Control) Control	Disabled	0x82

*For displaying custom images using the DVI input of the Pico module

4 Performance Information

Frame rate:

The Pico supports a frame rate of up to 60Hz. There are two supported modes 60Hz for NTSC and 50Hz Mode for PAL/SECAM.

Input options and resolution:

The selectable input modes are the splash screen mode, the internal test patterns, and the RGB mode which is the default setting for displaying still images or motion. The splash screens are stored as QVGA (320x240). When selected for use via an I²C or CPU bus command, a splash screen is automatically scaled to HVGA (480x320) and then displayed on the DMD. Test patterns fill the entire 480x320 DMD. For RGB input the resolution is VGA 640x480.

5 Subsystem

When data enters the DPP1505, the DPP1505 processes the digital input image and converts the data into a format that is needed by the DMD. Figure 3 below shows the data flow through the DPP1505.

Format Conversion:
The front end converts input data before it is ready to be processed. It transforms the input signal from one color space to another and changes data stream sampling. It is necessary to convert to an RGB color space so that RGB pixel values are sent to the DMD.

Image Enhancement:
This block supports up-scaling and down-scaling of input images with different resolutions and orientations. This part of the processor also applies a de-gamma function. The de-gamma correction function in this block cancels out the gamma function on incoming image frames. This block also performs Automatic gain control which boosts the brightness of darker scenes.

Artifact Mitigation:
This block enables the Temporal Enhance function, which extend the bit depth of the system for frame rates greater than 50Hz. Increased bit depth is needed to display the number of required color shades to accurately reproduce the low-level signals typical of most video sources. Increasing the overall bit depth resolution with this feature mitigates artifacts that would otherwise appear in video.

DMD Formatting:
This block formats data sent to the DMD. It also provides the interface to the external Mobile SDRAM. It handles the horizontal and vertical image flip function.

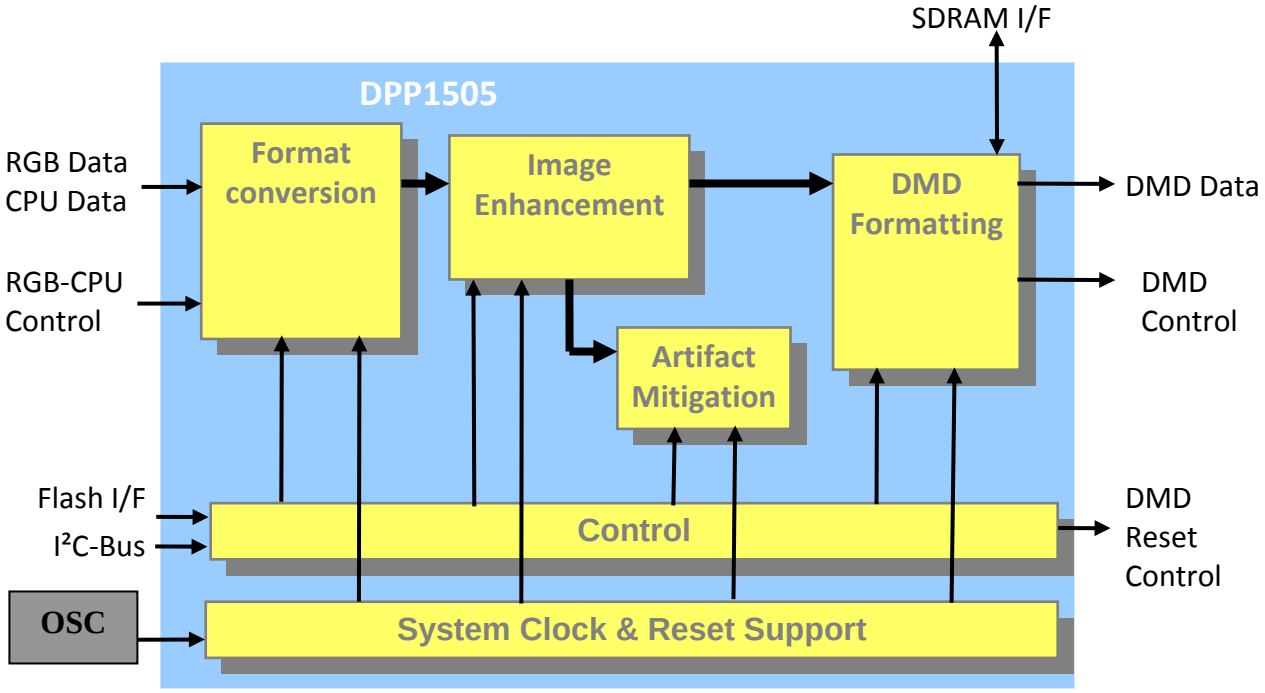


Figure 4: DDP1505 Internal Block Diagram